

DESIGN AND SIMULATION OF FLOATING POINT 32 INPUTS SPLIT-RADIX ALGORITHM

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ABSTRACT

Fast Fourier Transform plays a very important role in many engineering applications. Many different algorithms are proposed to improve the architecture of FFT among them Split-radix FFT is a particular FFT algorithm that aims to compute FFT with the least number of multiplications. The split-radix FFT mixes radix-2 and radix-4 decompositions, yielding an algorithm with about one-third fewer multiplies than the radix-2 FFT. The split-radix FFT has lower complexity than the radix-4 or any higher-radix power-of-two FFT. This paper proposes split-radix FFT for both real and floating point numbers. In this paper we use verilog for code implementation. The FPGA synthesis and logic simulation is displayed in Xilinx design suit13.2. The results shows the improvement in the speed

KEYWORDS: Split, Radix, Fast Fourier Transform, Butter Fly, Verilog, Floating Point, FPGA